READ CIRCUIT OF NONVOLATILE SEMICONDUCTOR MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS

[01] This application is a continuation of prior U.S. application serial no. 10/188,148, filed July 3, 2002, now Patent No. 6,674,668 which is a divisional of prior U.S. application serial no. 09/745,666, filed December 26, 2000, now Patent No. 6,438,638 which is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 11-373069, filed December 28, 1999, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[02] The present invention relates to a read circuit of a non-volatile semiconductor memory.

[03] 1. Types of Fast Random Accessible Nonvolatile Semiconductor Memories:

[04] As fast random accessible nonvolatile semiconductor memories, EEPROM, NOR cell type flash memory, and the like are known. In recent years, new types of memories based on a NAND cell type flash memory have been devised as a memory having a fast random access characteristic in parallel with these memories. One of such memories is a so-called "3Tr-NAND."

[05] The 3Tr-NAND is a memory which has each cell unit composed of three transistors, i.e., one memory cell and two select transistors sandwiching the memory cell, and has the following characteristics as compared with the EEPROM or flash memory:

[06] (1) ability of fast read in units of 16 bits (= word);

[07] (2) a small erasure unit of 32 words;

[08] (3) ability of performing a read operation at low power consumption; and

[09] (4) relatively small memory cell size.